I CLAIM:

1. A semiconductor device comprising:

a lower metal layer;

a lower dielectric layer on top of said lower metal layer;

an upper metal layer on top of said lower dielectric layer;

an upper dielectric layer on top of said upper metal layer;

a contact region formed as a cavity that extends through said upper dielectric layer, said upper metal layer and said lower dielectric layer for access to a solder pad portion of said lower metal layer;

a dielectric lining layer that lines a peripheral cavity-confining surface of said cavity and that is transverse to a plane of said lower metal layer to isolate said upper metal layer from said lower metal layer while permitting access to said solder pad portion of said lower metal layer; and

an electrical contact that fills said cavity and that enables external electrical connection with said lower metal layer.

2. The semiconductor device of Claim 1, further comprising a grounding trace that is disposed on said upper dielectric layer and that surrounds said cavity, said dielectric lining layer further extending on top of said upper dielectric layer to conceal said

grounding trace.

3. The semiconductor device of Claim 1, wherein said electrical contact is made from a conductive metal paste.

4. The semiconductor device of Claim 1, wherein said dielectric lining layer is made of a photoresist material.

5. A contact-forming method for a semiconductor device, the semiconductor device having a lower metal layer, a lower dielectric layer on top of the lower metal layer, an upper metal layer on top of the lower dielectric layer, an upper dielectric layer on top of the upper metal layer, and a contact region formed as a cavity that extends through the upper dielectric layer, the upper metal layer and the lower dielectric layer for access to a solder pad portion of the lower metal layer, said contact-forming method comprising:

forming the semiconductor device with a dielectric lining layer that lines a peripheral cavity-confining surface of the cavity and that is transverse to a plane of the lower metal layer to isolate the upper metal layer from the lower metal layer while permitting access to the solder pad portion of the lower metal layer; and

filling the cavity with a liquid metal to form an electrical contact that enables external electrical connection with the lower metal layer.

6. The contact-forming method of Claim 5, the semiconductor device further having a grounding trace that is disposed on the upper dielectric layer and that surrounds the cavity, wherein the dielectric lining layer extends on top of the upper dielectric layer to conceal the grounding trace.

7. The contact-forming method of Claim 5, wherein the liquid metal is a conductive metal paste.

8. The contact-forming method of Claim 5, wherein the step of forming the semiconductor device with the dielectric lining layer includes:

forming the dielectric lining layer on the upper dielectric layer such that the dielectric lining layer fills the cavity; and

removing a central portion of the dielectric lining layer from the cavity.

9. The contact-forming method of Claim 8, wherein the central portion of the dielectric lining layer is removed from the cavity with the use of a probe tool.

10. The contact-forming method of Claim 5, wherein the step of forming the semiconductor device with the dielectric lining layer includes:

filling a lining-forming hole in a steel plate with a dielectric material to form the dielectric lining layer; and

moving the dielectric lining layer from the steel plate to the semiconductor device.

11. The contact-forming method of Claim 10, wherein the dielectric lining layer is moved from the steel plate to the semiconductor device via a transfer printing unit.

12. The contact-forming method of Claim 8, wherein the dielectric lining layer is made of a photoresist material, and the step of removing the central portion of the dielectric lining layer from the cavity includes:

superimposing a patterned mask on the dielectric lining layer; and

exposing and developing the dielectric lining layer.